MEMORY ERROR DETECTING CORRECTING CIRCUIT

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Abstract of **JP61101857**

PURPOSE:To modify the content of an ROM, to easily modify the check code for error correction and to simplify the circuit configuration by performing the check bit generation and the correction detection of the memory error by using the ROM. CONSTITUTION:The information bit 14 from a CPU 11 is made an address data of a check bit generator ROM 12 and the content of the ROM 12 which the address represents is written in the ROM 12 beforehand so that it will be the data of a check bit 15. In this manner, the check bit 15 is generated. The check bit 15 and a data bit 14 from the CPU 11 are added to a memory 13. The information 14 read out from a memory 21 and a check bit 25 are added to a ROM for error detecting and correcting circuit 22, and a corrected information bit 26 and error correction flags 27 and 28 are outputted to a CPU 23. For each error detecting and correcting circuit and check bit generating circuit, a ROM in which expected output value corresponding to the input is written beforehand, is used respectively, and the content of said ROM is read out. In this way, the circuit configuration is simplified.